IN THE SPECIFICATION

Please replace the paragraph at page 27, prenumbered lines 18-28, with the following rewritten paragraph:

The silicon carbide vertical MOSFET having a low concentration gate region formed in a low concentration p-type deposition layer, in accordance with this invention, can be manufactured with a low ON-resistance and a high blocking voltage. The high blocking voltage of the silicon carbide vertical MOSFET is achieved by making the impurity concentration of a base region of a first conductivity type lower than that of a gate layer of a second conductivity type. The lowering of the ON-resistance is made possible by optimizing the impurity concentration of a portion of a second conductivity type in contact with the gate insulation film of a gate region of a second conductivity type selectively formed in a ~~second~~ deposition film.

Please replace the paragraph at page 27, prenumbered lines 29 to page 28, prenumbered line 2, with the following rewritten paragraph:

Also a high blocking voltage is imparted to the silicon carbide vertical MOSFET by optimizing the impurity concentration of a portion of a first conductivity type in contact with the high concentration gate region of a second conductivity type in the low concentration base region having a first conductivity type selectively formed in the ~~second~~ third deposition film.

Please replace the paragraph at page 28, prenumbered lines 15-21, with the following rewritten paragraph:

The ON-resistance is also be reduced without increasing the resistance in the vicinity of the interface between the gate insulation film and the low concentration base region of a

first conductivity type, by selectively forming the gate insulation film on the ~~second~~ third deposition film so that at least a portion thereof above the low concentration base region of a first conductivity type selectively formed in the second deposition film is thicker than the other parts of the region.

Please replace the paragraph at page 28, prenumbered lines 22-30, with the following rewritten paragraph:

The ON-resistance is also be reduced without increasing the resistance in the vicinity of the interface between the gate insulation film and the low concentration base region of a first conductivity type, by omitting at least part of the gate electrode formed on the surface of the base region of a first conductivity type selectively formed in the ~~second~~ third deposition film. Moreover, by using a substrate surface that is parallel to the (11-20) plane or (000-1) plane, the interface state density between the gate insulation film and the channel region is reduced, enabling a lower ON-resistance.

Please replace the paragraph at page 29, prenumbered lines 5-14, with the following rewritten paragraph:

The crystal quality of the ~~second~~ third deposition film deteriorates owing to the quality limit if the thickness is less than the lower limit of 0.2 μm, reducing electron mobility. Difficulties in the fabrication processes also limit the upper thickness of the film. Specifically, as shown in Figures 2(e) and 2(f) and Figures 5(e) and 5(f), the second region of a first conductivity type is formed by implantation of dopant ions of a first conductivity type from the surface of the deposition layer of a second conductivity type (by the so-called implantation for reverse), and if the film exceeds the maximum thickness of 0.7 μm, special ion implantation using very high energy is required, making it difficult to manufacture.